3DIC Thermal-Aware Early Design Optimization

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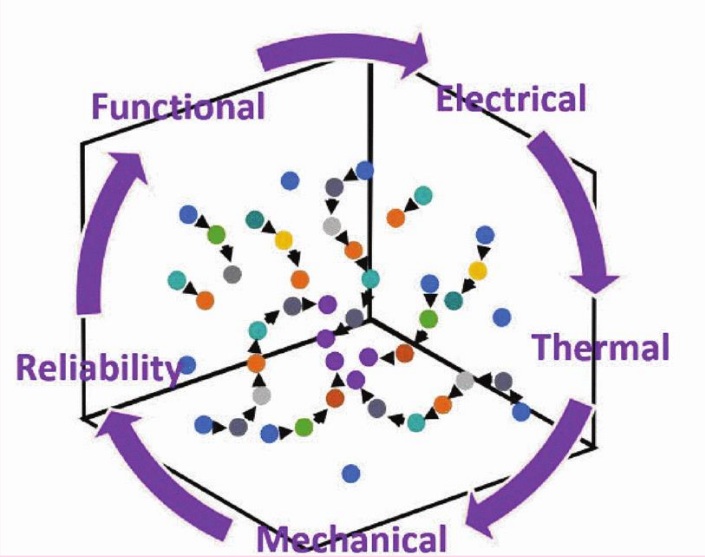
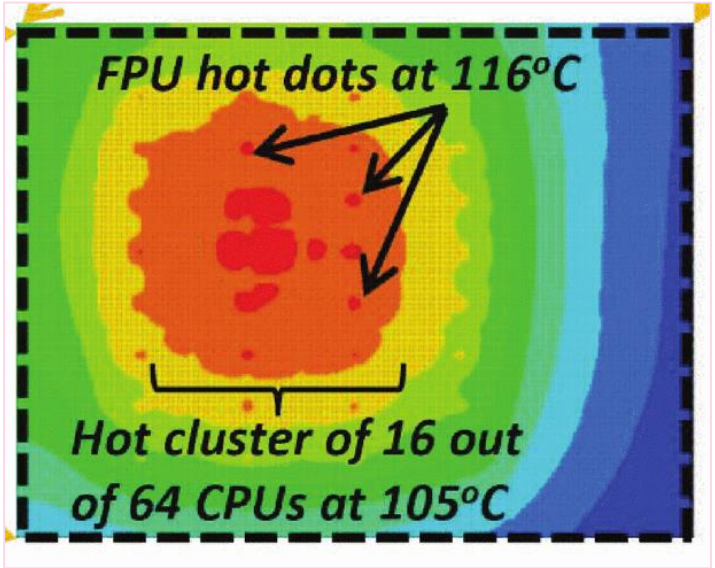
Motivation

- **3DIC Demands More on Thermal Management**
  - Deign with poor thermal management degrades product performance and reduces its service lifetime
  - Multi-chiplets and stacks in 2.5D and 3D configuration calls for much earlier thermal assessment in system planning phase
  - Addressing thermal challenges in later stage of design can drastically increase overall design cycle time
  - Lack of well-defined thermal and PPA co-optimization in the current implementation tool chains
- **Early thermal analysis unveils new avenues**
  - 'Pre-placement thermal simulation' + 'concurrent 3D design' unlock early optimization opportunities
  - Must have new tool sets that can address 3DIC system design and integrate with thermal and power design in early phase
- **Novel methodology: thermal-aware early design optimization**
  - Integrity_3dic and Celsius tools are designed to tackle the complex design needs
  - Convert thermal results to calculated module spacing in design
  - Iterating module floorplanning in 3D databases to achieve balanced thermal/PPA metrics



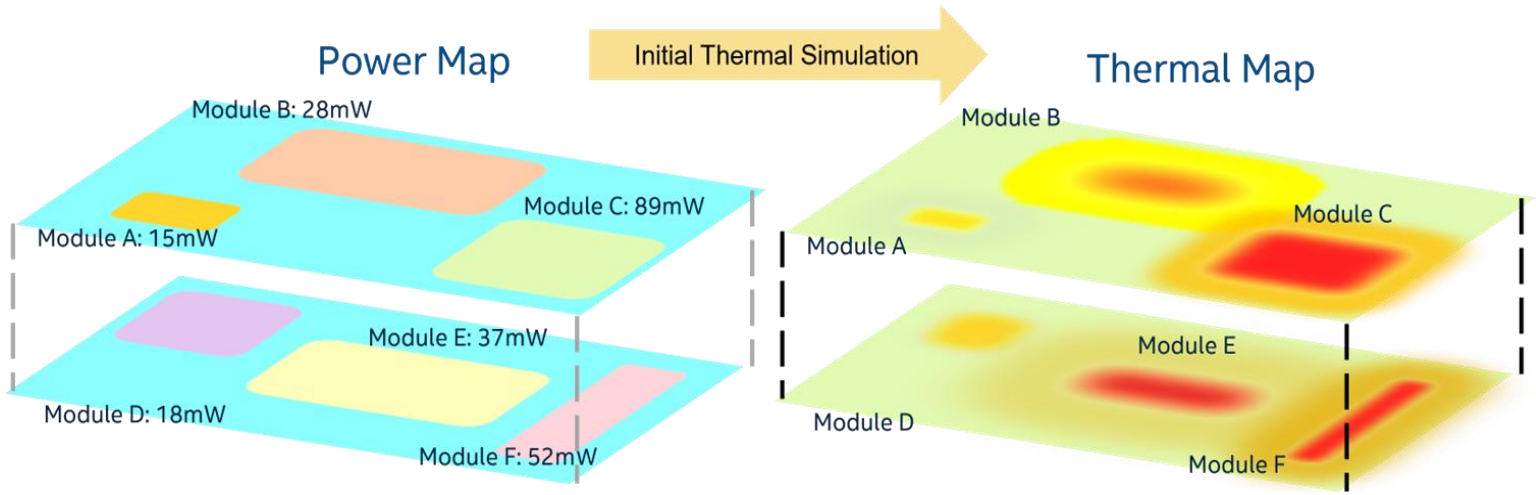


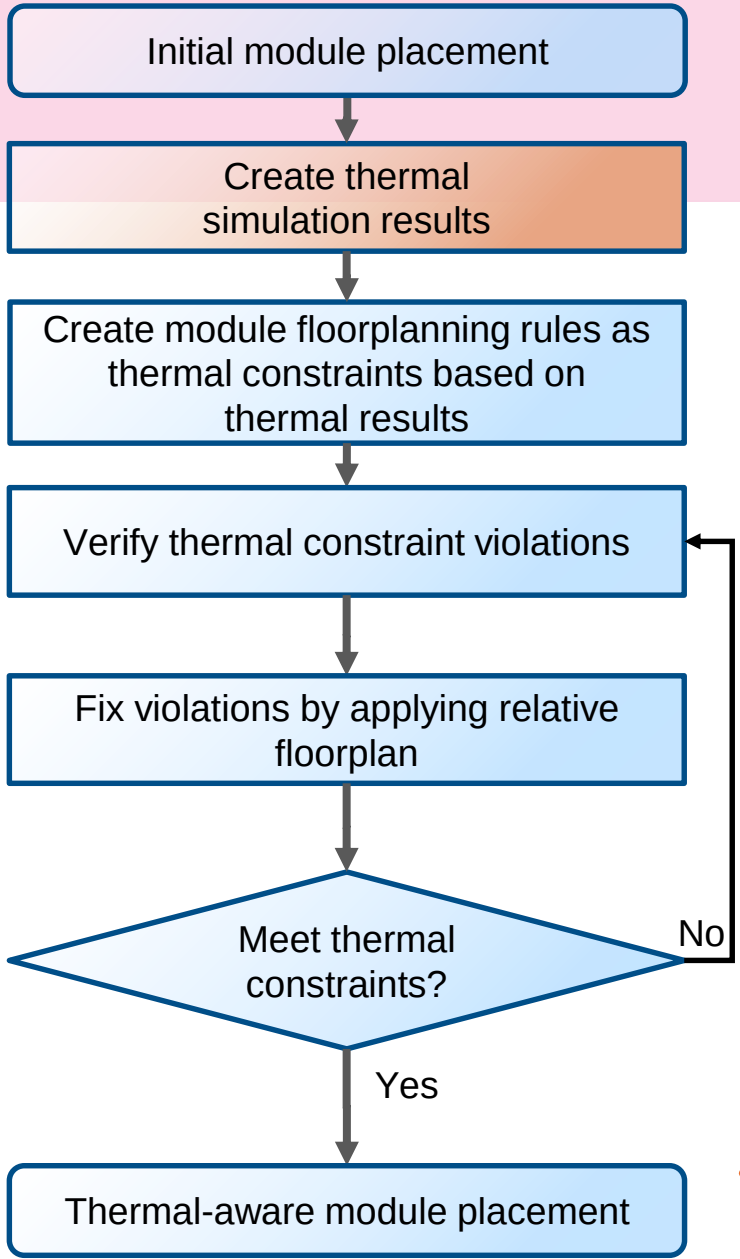
Source: 2024 IEEE Symposium on VLSI Technology and Circuits

Main Idea:
Thermal-aware Early Design Optimization

- **Proposed Solution**
  - Thermal simulation results of initial module placement guide the thermal constraint creation of P&R stage.
  - Thermal constraints guide module floorplanning of early design optimization.
  - Verify and fix the thermal constraints violations iteratively at P&R stage without thermal simulation quickly converge the thermal impact and module floorplanning.
  - The solution models the thermal impact for early design optimization and shorten the design cycle between implementation and thermal verification.

Thermal-aware Early Design Optimization





P&R Implement *(Cadence Integrity 3DIC)*

Thermal Simulation *(Cadence Celsius)*

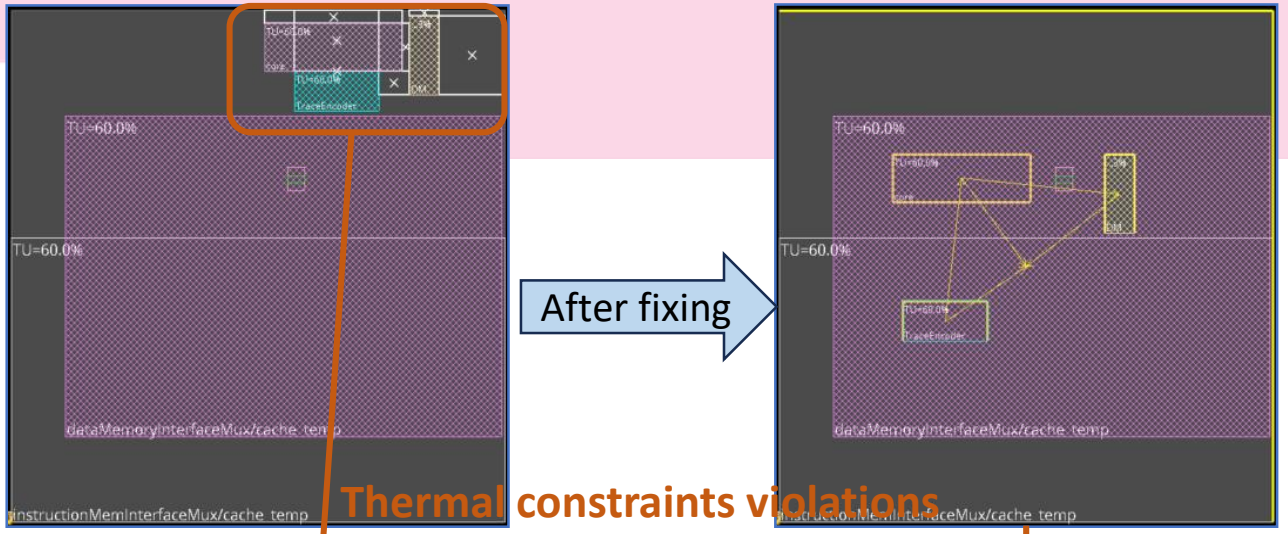
Thermal-aware Early Design Optimization

- **Thermal constraints creation**
  - Mapping initial thermal simulation results to module floorplan constraints.
  - Putting high power modules away from the chip boundary as far as possible.
  - Improve unit area heat by setting spacing rules between high-power modules in both 2D and 3D.
  - Apply the constraints and show the violation.
- **Fixing the constraints violations**
  - Apply relative floorplan for modules and automatically fix the violations

Thermal Constraints Examples:

set_spacing_rule -name thermal_constraints_bndry -obj [design boundary] -ref [module bounding box] -direction all {.spacing >= <space>} -description {thermal violation between module and design boundary} -enclosure

set_spacing_rule -name thermal_constraints_sp -obj [module A bounding box] -ref [module B bounding box] -direction all {.spacing >= <space>} -description {thermal violation between modules} -no_overlap




```
checking rule : thermal_constraints_bndry_0
checking rule : thermal_constraints_bndry_1
checking rule : thermal_constraints_bndry_2
checking rule : thermal_constraints_sp_0
checking rule : thermal_constraints_sp_1
checking rule : thermal_constraints_sp_2
-------------- Summary of UFC Checking --------------
RuleName                    Count     Description     ViolatedObjects
........                    .....     ...........     ...............
thermal_constraints_bndry_0   2       thermal violation between hInsts DM and design boundary       {{187.25 193.44 201.15 229.2}
}
thermal_constraints_bndry_1   1       thermal violation between hInsts TraceEncoder and design boundary      {{133.25 186.0 173.0
204.0}}
thermal_constraints_bndry_2   1       thermal violation between hInsts core and design boundary      {{119.0 204.24 183.9 225.84}}
thermal_constraints_sp_0      1       thermal violation between hInsts core and TraceEncoder  {{119.0 204.24 183.9 225.84}}
thermal_constraints_sp_1      1       thermal violation between hInsts core and DM    {{119.0 204.24 183.9 225.84}}
thermal_constraints_sp_2      1       thermal violation between hInsts TraceEncoder and DM    {{133.25 186.0 173.0 204.0}}
        Finished checking thermal constraints.tcl
```

After fixing

Meet thermal constraints

```
checking rule : thermal_constraints_bndry_0
checking rule : thermal_constraints_bndry_1
checking rule : thermal_constraints_bndry_2
checking rule : thermal_constraints_sp_0
checking rule : thermal_constraints_sp_1
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```
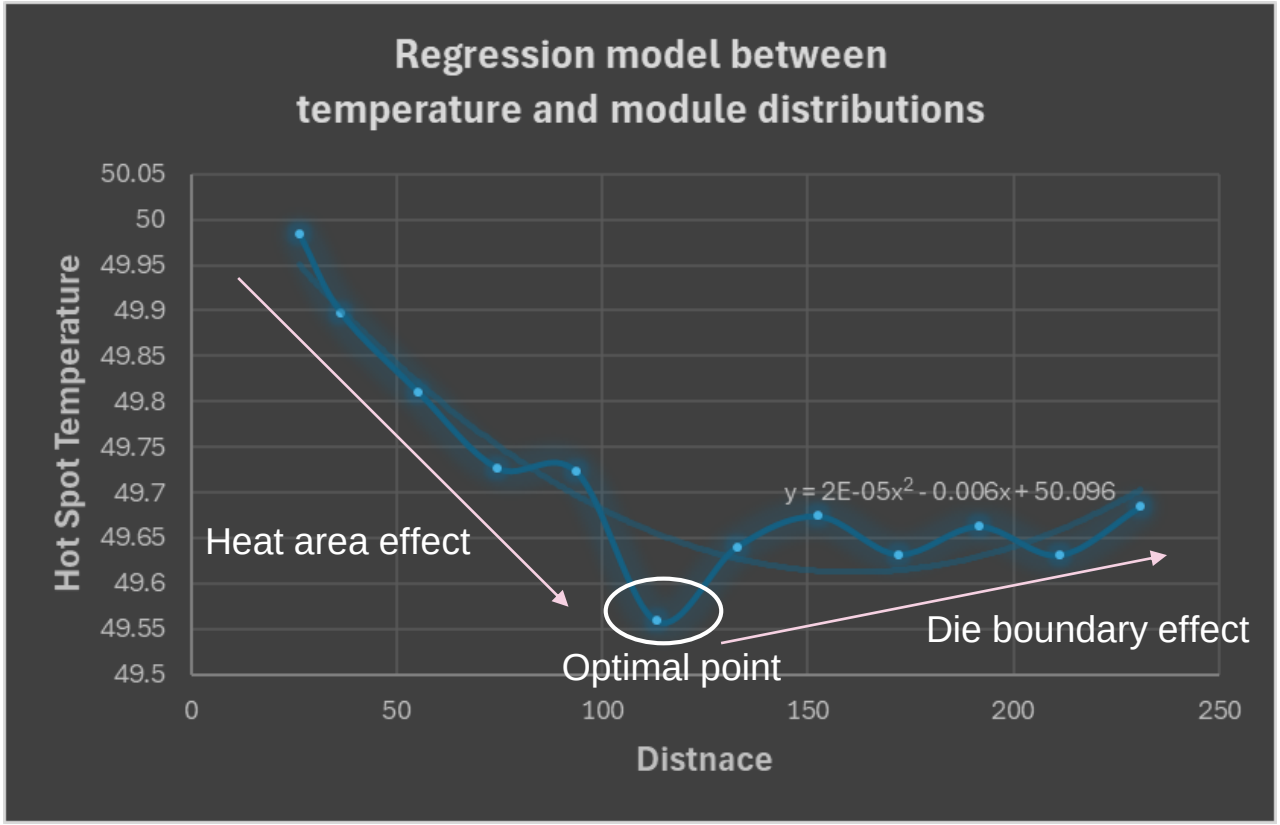
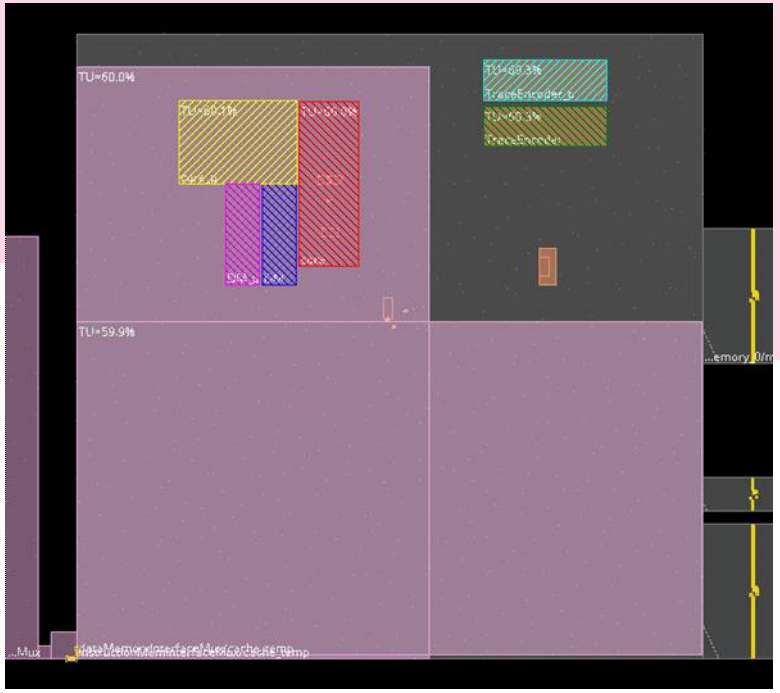

Thermal-aware Early Design Optimization

- **Thermal constraints regression model**
  - The regression model is based on the technology node and system vehicle.
  - The die boundary and heat area effects are modeled.
  - The model provides the guidance between module placement and optimal hot spot temperature.
  - Thermal constraints can be created based on the model.

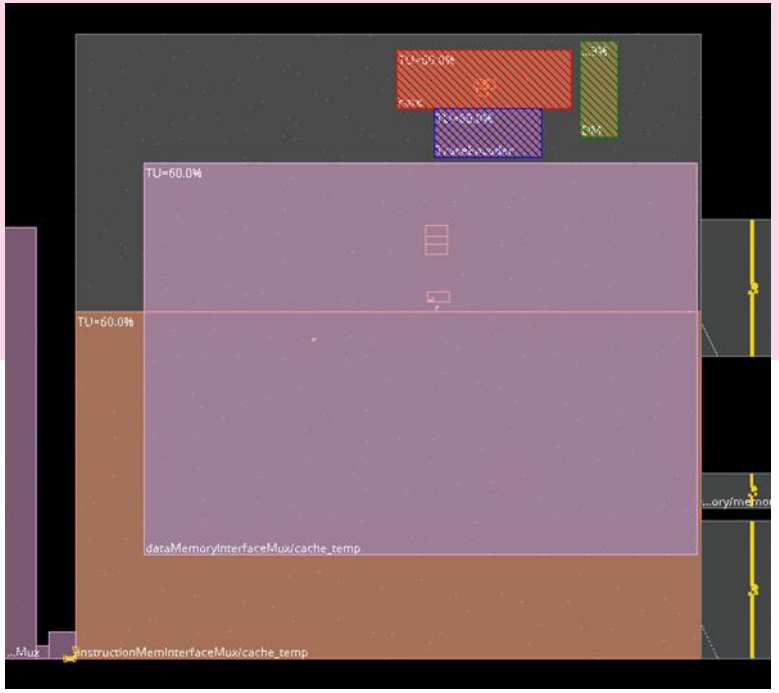


Evidence

- **Validate the solution with different testcases**
  - Different total power, modules numbers and physical distribution of testcases show the flow scalability
  - Design #1 - Results showcase as (a)
  - Design #2 - Results showcase as (b),(c) and (d)
  - Demonstrate automatically thermal-aware module placement

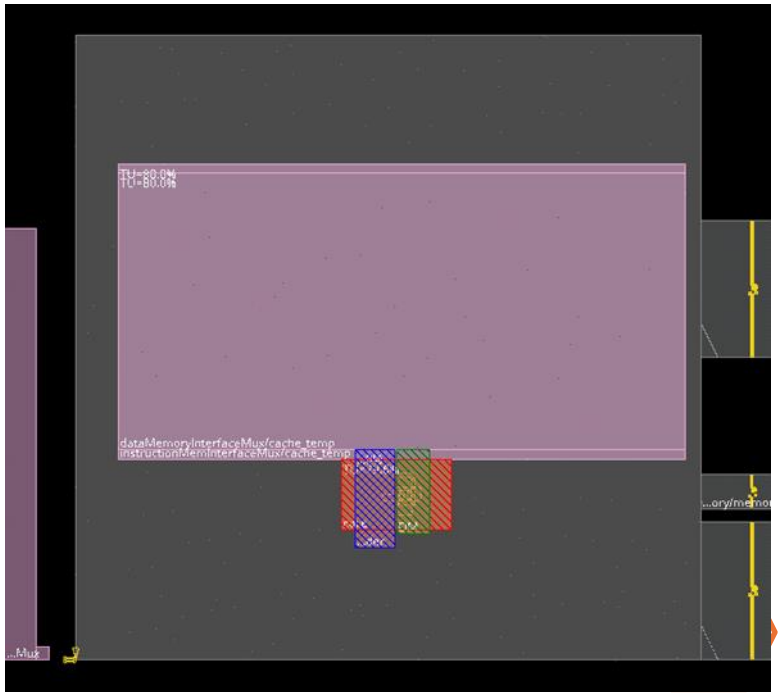


(a)



(b)

(c)



(d)

Evidence

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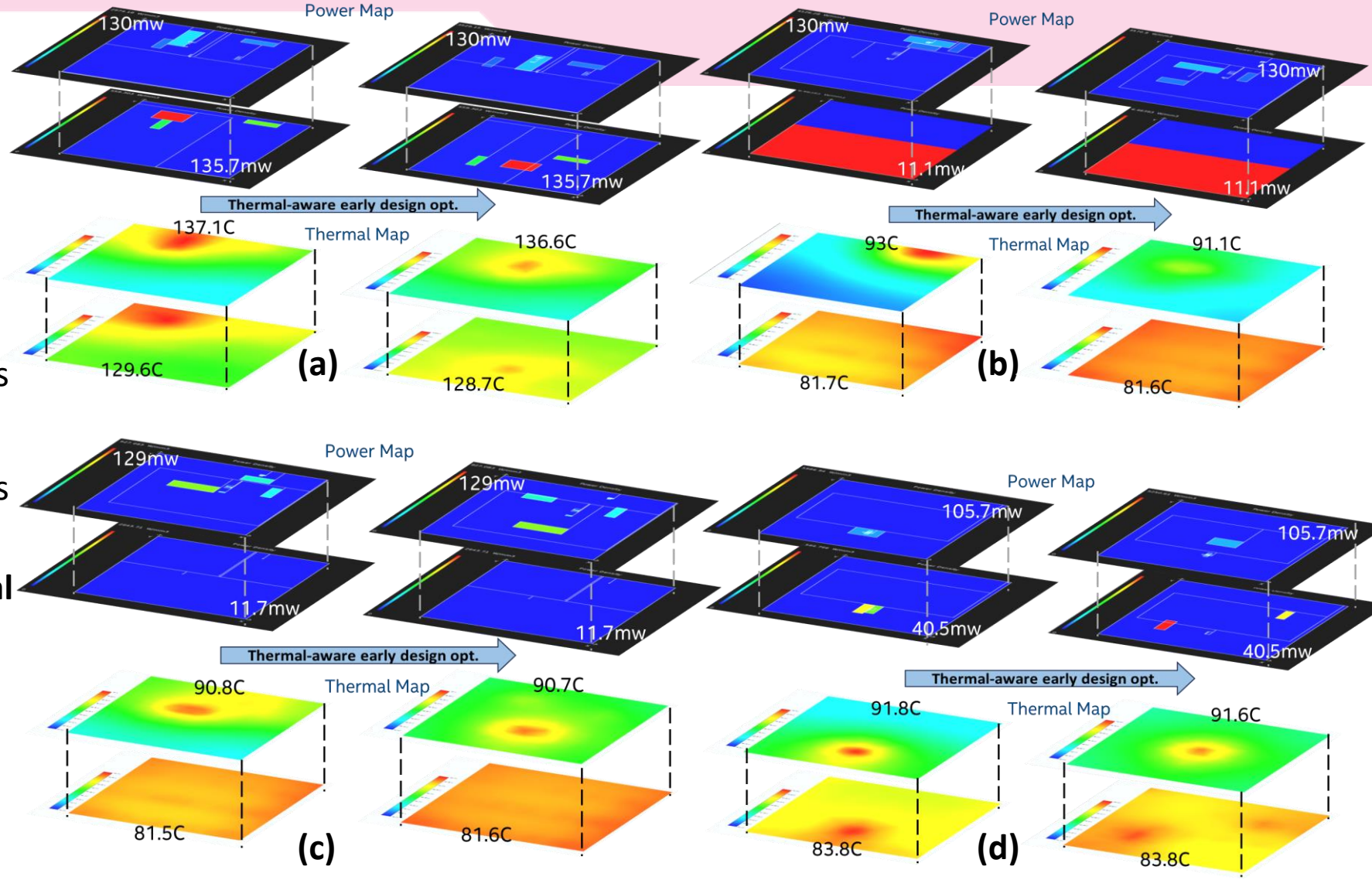
- **The results showcase the thermal are improved in either of the following conditions**
  - Max temperature improved
  - Better thermal distribution within die



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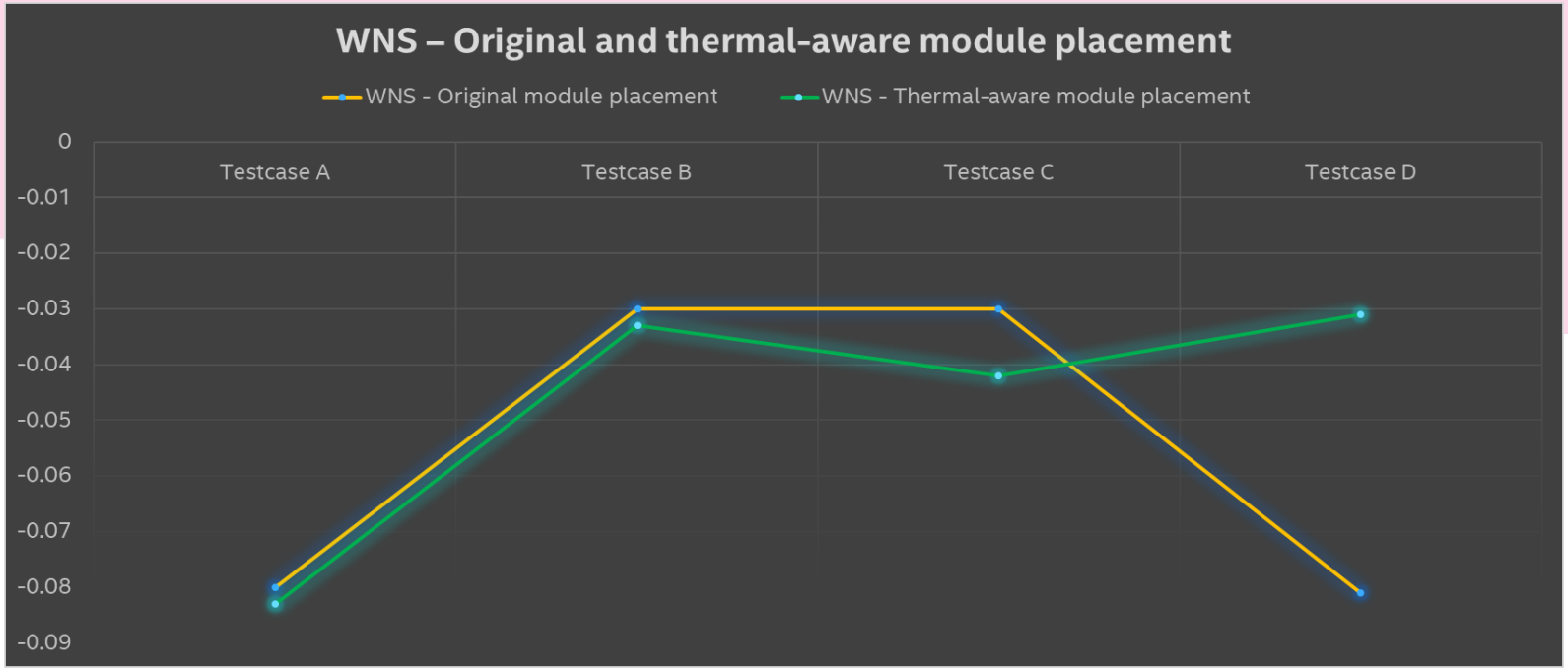
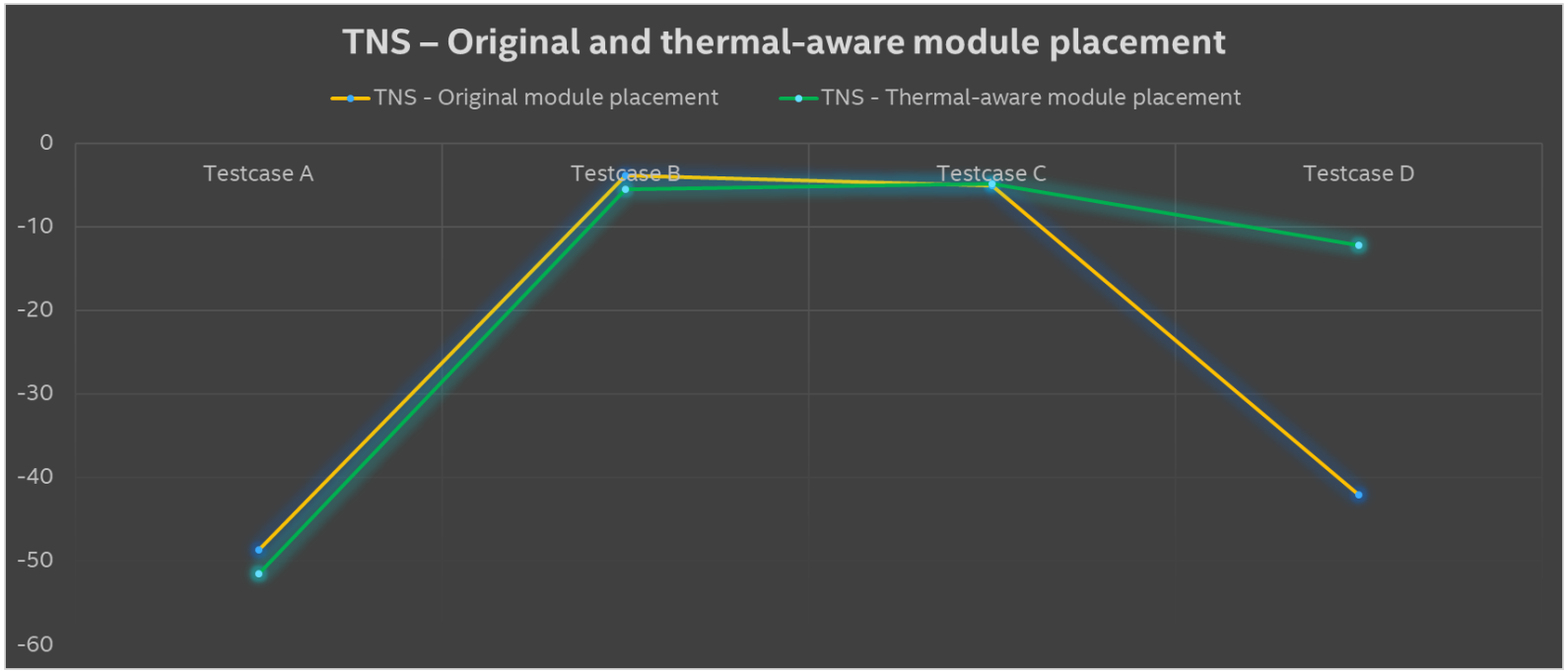
  - Timing results are comparable between original and thermal-aware module placement





Summary & Next Steps

- “First Generation” thermal-aware early design optimization and experiments (based on Cadence Integrity 3DIC platform and Celsius)
  - Modeling thermal constraints at early design stage
  - Convert the thermal simulation results to actionable module spacing rules
  - Applying relative floorplanning by setting floorplan constraints between modules
  - Quick turnaround to resolve thermal issues and achieve PPA goal

- Call to Action
  - Exploring different thermal profiles of different designs enhances the algorithm and formula of automatic thermal constraints fix.
  - Many options for each thermal constraints would need to be considered with physical implementation tradeoffs.
  - Leverage ML/AI techniques to explore thermal and PPAC tradeoffs